Inventor Information for 10/528607

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Application# Title	Patent#	Status	Date Filed
10596336 BLOCK CIPHERING SYSTEM, USING PERMUTATIONS TO HIDE THE CORE CIPHERING FUNCTION OF EACH ENCRYPTION ROUND	Not Issued	20	06/09/2006
09734773 DATA PROCESSOR UITILIZING SET-ASSOCIATIVE CACHE MEMORY FOR STRREAM AND NON-STREAM MEMORY ADDRESSES	6643738	150	12/12/2000
09981135 INTERRUPTIBLE DIGITAL SIGNAL PROCESSOR HAVING TWO INSTRUCTION SETS	7082518	150	10/16/2001
11568714 LOWER POWER ASSEMBLER	Not Issued	19	01/01/0001
12264085 METHOD AND APPARATUS FOR DESIGNING A PROCESSOR	Not Issued	19	11/03/2008
60984593 METHOD AND APPARATUS FOR DESIGNING A PROCESSOR	Not Issued	159	11/01/2007
11577829 METHOD AND SYSTEM FOR OBFUSCATING A CRYPTOGRAPHIC FUNCTION	Not Issued	20	04/24/2007
10274400 METHOD OF ENHANCING THE SECURITY OF A PROTECTION MECHANISM	Not Issued	161	10/18/2002
11573816 PROCESSING APPARATUS WITH BURST READ WRITE OPERATIONS	Not Issued	93	12/21/2007
10524535 PROCESSING APPARATUS, PROCESSING METHOD AND COMPILER	7313671	150	02/10/2005
10528607 PROCESSING APPARATUS, PROCESSING METHOD AND COMPILER	Not Issued	71	03/21/2005

10541275   Not Issued   71   06/30/2005
PROCESSING SYSTEM INCLUDING RECONFIGURABLE CHANNEL INFRASTRUCTURE FOR EFFICIENT
CLUSTERING OF PROCESSING ELEMENTS

10515463   7231478   150   11/22/2004
PROGRAMMED ACCESS LATENCY IN MOCK MULTIPORT MEMORY

10515453   7308540   150   11/22/2004
PSEUDO MULTIPORT DATA MEMORY HAS STALL FACILITY

10511512   Not Issued   121   10/14/2004
REGISTER SYSTEMS AND METHODS FOR A MULTI-ISSUE PROCESSOR

09969094   6948158   150   10/02/2001
RETARGETABLE COMPILING SYSTEM AND METHOD

11568984   Not Issued   61   11/13/2006
RUN-TIME SELECTION OF FEED-BACK CONNECTIONS IN A MULTIPLE-INSTRUCTION WORD
PROCESSOR

08963932   6049818   150   11/04/1997
SIGNAL PROCESSING DEVICE

10016184   7032102   150   12/10/2001
SIGNAL PROCESSING DEVICE AND METHOD FOR SUPPLYING A SIGNAL PROCESSING RESULT TO A
PLURALITY OF REGISTERS

09174166   6400410   150   10/16/1998
SIGNAL PROCESSING DEVICE AND METHOD OF PLANNING CONNECTIONS BETWEEN PROCESSORS
IN A SIGNAL PROCESSING DEVICE

10526421   Not Issued   41   03/01/2005
STACK TYPE SNAPSHOT BUFFER HANDLES NESTED INTERRUPTS

10552767   Not Issued   41   10/12/2005
SUPPORT FOR CONDITIONAL OPERATIONS IN TIME-STATIONARY PROCESSORS

10059427   Not Issued   124   01/29/2002
VARIABLE LENGTH VLIW INSTRUCTION WITH INSTRUCTION FETCH CONTROL BITS FOR
PREFETCHING, STALLING, OR REALIGNING IN ORDER TO HANDLE PADDING BITS AND
INSTRUCTIONS THAT CROSS MEMORY LINE BOUNDARIES

10554621   7302555   150   10/27/2005
ZERO OVERHEAD BRANCHING AND LOOPING IN TIME STATIONARY PROCESSORS